Hybrid Switched-Capacitor/Switched-Quasi-Z-Source Bidirectional DC-DC Converter With Wide-Voltage-Gain Range for Hybrid Energy Sources EVs

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***Abstract*—In this paper, a hybrid switched-capacitor/ switched-quasi-Z-source bidirectional dc-dc converter is proposed for electric vehicles (EVs) with hybrid energy sources, which has a wide voltage gain range in the bidirectional energy flows. Compared with the traditional quasi-Z-source bidirectional dc-dc converter, the proposed converter only changes the position of the main power switch, and employs a switched-capacitor cell at the output of the high voltage side. Therefore, the advantages of the wide voltage gain range and the lower voltage stresses across the power switches can be achieved. The operating principle, the voltage and current stresses across the power switches and the comparisons with other converters are analyzed in detail. Furthermore, the parameter design of the main components, the dynamic modelling analysis and the voltage control scheme are also presented. Finally, the experimental results obtained from a 400W prototype validate the characteristics and the theoretical analysis of the proposed converter.**

***Index Terms*—Bidirectional dc-dc converter, electric vehicles (EVs), hybrid energy sources, switched-capacitor, switched- quasi-Z-source, wide voltage gain range.**

I. Introduction

With the rapid development of power electronics, bidirectional dc-dc converters have been widely used in micro-grids, renewable energy systems, electric vehicles (EVs) and other applications to ensure the power flows from, to or between various energy storage devices. Therefore, these bidirectional dc-dc converters, which interface the energy storage devices and the dc bus with different voltage levels, have recently become an important research spot [1], [2].

In many cases, a wide voltage gain range between the low voltage and high voltage sides is required for the bidirectional dc-dc converters [3], [4]. In terms of EVs with hybrid energy sources, the bidirectional dc-dc converters play an important role in controlling the voltage of the dc bus and maintaining the power balance of the whole system. The hybrid energy sources of EVs are mainly comprised of high energy density power batteries and high power density super-capacitors. The voltage levels of hybrid energy sources, especially the super-capacitor bank, are relatively low. In order to make full use of the energy source capacities and match the voltage levels between the hybrid energy sources and the high voltage dc bus, a bidirectional dc-dc converter with wide voltage gain range is needed to interface the energy sources and the onboard dc bus [5].

In some applications, dc-dc converters are required to achieve the galvanic isolation and the high voltage gain. Therefore, the Fly-back, forward or full bridge phase shifted dc-dc converters can often be used. When the galvanic isolation is not required, the traditional bidirectional buck/boost dc-dc converter can be applied when power flows in both directions are required. Other standard bidirectional dc-dc converters can also be applied in various energy storage systems. Each converter has its own advantages and disadvantages in terms of the voltage gain, the component count and the voltage stress [6]. By adding additional capacitors and power switches, the conventional buck/boost converter can be improved to the three level [7], four level [8] or multilevel converters [9] for a wider operation range of the higher voltage gain. However, the multilevel dc-dc converters need more power switches, additional hardware circuits and control strategies to maintain the balance of the voltage stresses across the power switches and capacitors. Other known dc-dc converters, such as Cuk/Sepic/Zeta converters, can also be modified into bidirectional topologies, but these unique structures may limit the efficiencies of the converters [10]-[12].

In addition, when additional switched-capacitor or switched-inductor is added into buck/boost or other simple structure converters, they can be retrofitted into non-isolated hybrid dc-dc converters, which can also achieve a higher voltage gain [13], [14]. The structures of Z-source, quasi-Z-source and switched-capacitor dc-dc converters are simple and easy to expand, and the capacitors in these converters deliver energy through different paths during the

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charging and the discharging processes, so as to achieve high voltage gain [15]-[18]. A switched-quasi-Z-source converter, derived from the traditional quasi-Z-source converter, has been proposed in [19], as shown in Fig. 1. However, the voltage gain of the switched-quasi-Z-source converter is still limited, and the power switches suffer from higher voltage stresses. Switched-inductor dc-dc converters can achieve the wide voltage gain ranges and lower voltage stresses across the power switches at the expense of the lower power densities [20], [21].

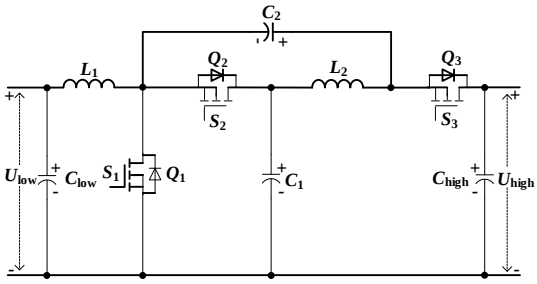


Fig. 1 Switched-quasi-Z-source converter in [19]

Based on the switched-capacitor converters and the switched-quasi-Z-source converter in [19], a novel hybrid switched-capacitor/switched-quasi-Z-source bidirectional dc-dc converter for EVs with hybrid energy sources is proposed in this paper. The proposed converter only employs two extra power switches and capacitors compared to that in [19]. Then, it achieves a wide voltage gain range, also has the low voltage stresses across the power switches. In addition, the voltage gain of the proposed converter is wide enough to meet the operation requirements of the hybrid energy sources EVs, especially the proposed converter can act as a power interface between the onboard dc bus and the low voltage super-capacitor bank.

The hybrid energy sources system of an EV that incorporates the proposed converter is shown in Fig. 2. Its power could be tens of kilowatt (kW) and belongs to the medium power level. The whole system mainly includes a super-capacitor bank, a battery pack, a traditional bidirectional dc-dc converter and the proposed bidirectional dc-dc converter. The cost analysis of the two types of energy sources, including the hybrid energy sources system previously referred and the traditional energy source system with the single battery pack, is given in TABLE I. As shown in TABLE I, the equipment cost gap between these two kinds of energy sources systems tends to be smaller, due to the reducing cost of super-capacitor bank. The total cost of the above hybrid energy sources system may be smaller than that of the energy source system with the single battery pack [22]-[24]. Therefore, the hybrid energy sources EVs would have a good application prospect in the aspect of the cost. The battery pack is often configured with a number of cells in series to achieve a higher voltage, so as to maintain the dc bus voltage through a traditional bidirectional dc-dc converter during the steady state, even when the required energy has low-frequency fluctuations. However, the output voltage of the super-capacitor bank has a wide voltage range. Hence, a wide voltage gain range bidirectional dc-dc converter, such as the proposed bidirectional dc-dc converter, is required as a power interface between the high voltage dc bus and the low voltage super-capacitor bank. The super-capacitor bank can provide or absorb high-frequency instantaneous power during the EVs' starting, accelerating, decelerating or braking processes. Thus, these two hybrid energy sources can greatly reduce the degradation impact on the batteries caused by the sudden load change of EVs, and also improve the dynamic response of the whole hybrid energy sources system [25], [26].

The remainder of this paper is structured as follows. Section II introduces the configuration and analyzes the operating principle of the proposed converter in detail. The parameter design of the proposed converter is presented in Section III. The experimental results and analysis are shown in Section IV, and Section V gives the conclusions.

TABLE I
COST ANALYSIS OF ENERGY SOURCE SYSTEM

Energy Source System	Equipment cost	Operating cost	Post-maintenance cost
Energy source with single battery pack	Low	High	High
Energy sources with battery pack and super-capacitor bank	High	Low	Low

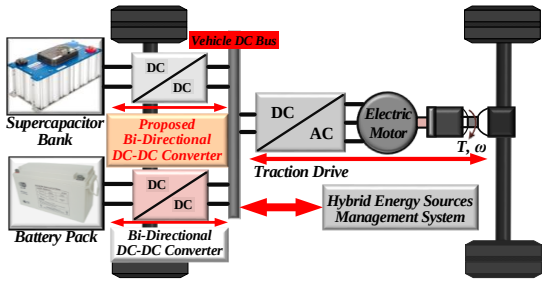


Fig. 2 Hybrid energy sources system of an EV.

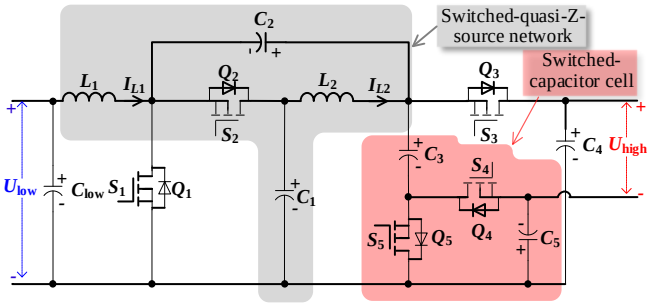


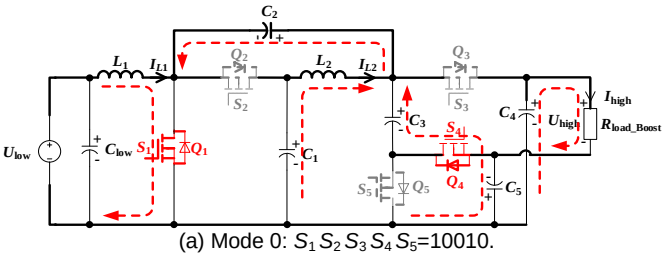
Fig. 3 Configuration of the proposed converter.

II. OPERATING PRINCIPLE AND ANALYSIS OF THE PROPOSED CONVERTER

The configuration of the proposed converter is depicted in Fig. 3. As shown in Fig. 3, the proposed converter mainly includes a switched-quasi-Z-source network (L_1, L_2, C_1, C_2 and Q_2) and a switched-capacitor cell (C_3, C_5, Q_4 and Q_5). The gate signals S_2, S_3 and S_5 for Q_2, Q_3 and Q_5 are identical, and they are complementary to the gate signals S_1 and S_4 which control Q_1 and Q_4 respectively. U_{low} is normally a low voltage source, which is usually comprised of the hybrid energy sources, such as a battery pack or a super-capacitor bank. U_{high} is a high voltage source that represents a 400V dc bus of the EV with hybrid energy sources in the application considered in this paper. The power switch adopted in the proposed converter is a MOSFET with an anti-parallel diode. When the power switch is forward turned on, the forward current flows through the MOSFET. When the power switch operates in the reverse conduction, the reverse current not only flows through the body diode, but also flows through the MOSFET under the synchronous rectification condition to reduce the conduction losses of the power switches, so as to improve the overall efficiency of the converter.

Compared with the switched-quasi-Z-source dc-dc converter in [19], as shown in Fig. 1, the proposed converter only employs a switched-capacitor cell, including two power switches and two capacitors, at the output of the high voltage side. Therefore, the advantages of the wider voltage gain range and the lower voltage stresses across the power switches can be obtained.

In order to simplify the analysis of the proposed converter, it is assumed that the ON-STATE resistances of the power switches and the parasitic resistances of the inductors and the capacitors are ignored, and the currents of the inductors and the voltages of the capacitors increase and decrease linearly.



(a) Mode 0: $S_1S_2S_3S_4S_5$=10010.

(b) Mode 1: $S_1S_2S_3S_4S_5$=01101.

Fig. 4 Equivalent circuits of the proposed converter in step-up mode.

A. Step-Up Mode of the Proposed Converter

The proposed converter in the step-up mode is shown in Fig. 4, and the typical waveforms of the proposed converter in the continuous conduction mode (CCM) are illustrated in Fig. 5 (a). In this operating mode, Q_1 operates as a main power switch, and Q_2-Q_5 are the complementary power switches. The steady-state analysis is described as follows.

***Mode 0*:** During the interval [t_0-t_1], Q_1 is forward turned on, Q_4 is reversely turned on and Q_2, Q_3 and Q_5 are turned off. As shown in Fig. 4 (a), L_1 is charged by U_{low} through Q_1, while C_1 discharges, and the energy is transferred to C_2 and L_2 through Q_1. C_3 charges C_2 and C_5. Meanwhile, C_4 also charges C_2 and provides the energy for the load R_{load_Boost}.

***Mode 1*:** During the interval [t_1-t_2], Q_1 and Q_4 are turned off, and Q_2, Q_3 and Q_5 are reversely turned on. As shown in Fig. 4 (b), the input voltage U_{low} and L_1 charge C_1 through Q_2. C_2 is connected in parallel with L_2, while connected with U_{low} and L_1 in series to charge C_4. C_5 is connected in series with C_2 and U_{low} to supply the energy for the load R_{load_Boost}.

B. Step-Down Mode of the Proposed Converter

In the step-down mode, the proposed converter acts as a charger, namely the power is taken from the high-voltage source U_{high} to the low-voltage source U_{low}. In this operating mode, Q_2-Q_5 operate as the main power switches, and Q_1 is the complementary power switches. The typical waveforms of the proposed converter in CCM are shown in Fig. 5 (b). Fig. 6 illustrates the current flow paths in one switching period. The steady-state analysis is described as follows.

***Mode 0*:** During the interval [t_0-t_1], Q_1 and Q_4 are turned off, and Q_2, Q_3 and Q_5 are turned on. As shown in Fig. 6 (a), L_1, L_2 and C_2 are charged by C_3, C_4 and U_{high}, and C_1 charges L_1. Meanwhile, C_4 and C_1 and the high-voltage source U_{high} supply energy for the load R_{load_Buck}, and C_5 is also charged by U_{high}.

***Mode 1*:** During the interval [t_1-t_2], Q_1 is forward turned on, Q_4 is reversely turned on and Q_2, Q_3 and Q_5 are turned off. As shown in Fig. 6 (b), C_4 and C_3 are charged by U_{high}, while C_2 is connected in series with L_2 to charge C_1 through Q_1. C_5 is connected in series with C_2 to charge C_3. L_1 also supplies energy for the load R_{load_Buck} through Q_1.

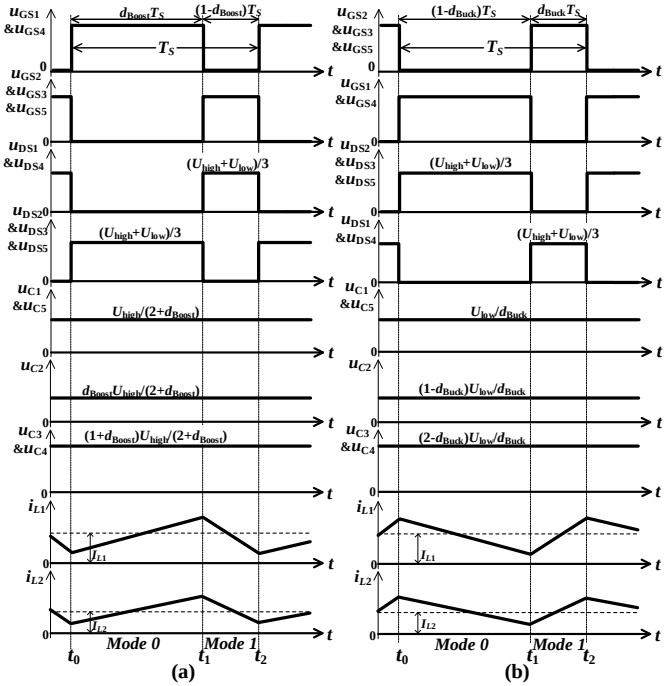
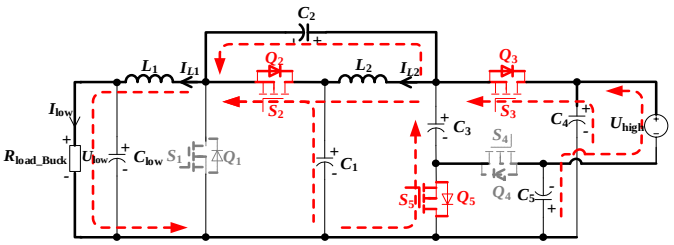


Fig. 5 Typical waveforms of the proposed converter. (a) Step-up mode. (b) Step-down mode.



(a) Mode 0: $S_1S_2S_3S_4S_5$=01101.

(b) Mode 1: $S_1S_2S_3S_4S_5$=10010.

Fig. 6 Equivalent circuits of the proposed converter in step-down mode.

C. Analysis of Steady State Characteristics

1. Steady-State Analysis in the Step-Up mode

According to Fig. 4 (a) and (b) and the volt-second balance principle on inductors L_1 and L_2, the following equations can be obtained:

$$\begin{cases} d_{Boost}\cdot U_{low}+(1-d_{Boost})\cdot(U_{low}-U_{C1})=0 \\ d_{Boost}\cdot(U_{C1}-U_{C2})+(1-d_{Boost})\cdot(U_{C1}-U_{C4})=0 \end{cases} \quad (1)$$

$$\begin{cases} U_{\text{high}} = U_{\text{C4}} + U_{\text{C5}} \\ U_{\text{C5}} + U_{\text{C2}} = U_{\text{C3}} \\ U_{\text{C5}} = U_{\text{C1}} \\ U_{\text{C3}} = U_{\text{C4}} \end{cases} \tag{2}$$

where d_{Boost} is the duty cycle of Q_1 and Q_4 of the proposed converter in the step-up mode.

Therefore, by simplifying (1) and (2), the voltage stresses across C_1-C_5 in the step-up mode can be obtained as:

$$\begin{cases} U_{\text{C1\_Boost}} = U_{\text{C5\_Boost}} = \dfrac{U_{\text{low}}}{1-d_{\text{Boost}}} = \dfrac{U_{\text{high}}}{2+d_{\text{Boost}}} \\ U_{\text{C2\_Boost}} = \dfrac{d_{\text{Boost}}U_{\text{low}}}{1-d_{\text{Boost}}} = \dfrac{d_{\text{Boost}}U_{\text{high}}}{2+d_{\text{Boost}}} \\ U_{\text{C3\_Boost}} = U_{\text{C4\_Boost}} = \dfrac{(1+d_{\text{Boost}})U_{\text{low}}}{1-d_{\text{Boost}}} = \dfrac{(1+d_{\text{Boost}})U_{\text{high}}}{2+d_{\text{Boost}}} \end{cases} \tag{3}$$

and the voltage stresses across Q_1-Q_5 in the step-up mode can also be written as:

$$\begin{aligned} U_{Q_1\text{\_Boost}} &= U_{Q_2\text{\_Boost}} = U_{Q_3\text{\_Boost}} = U_{Q_4\text{\_Boost}} \\ &= U_{Q_5\text{\_Boost}} = \frac{U_{\text{high}}}{2+d_{\text{Boost}}} = \frac{U_{\text{high}}+U_{\text{low}}}{3} \end{aligned} \tag{4}$$

Substituting (3) into (2), the voltage gain G_{Boost} (in CCM) of the proposed converter in the step-up mode can be expresses as:

$$G_{\text{Boost}} = \frac{2+d_{\text{Boost}}}{1-d_{\text{Boost}}} \tag{5}$$

2. Steady-State Analysis in the Step-Down mode

In the similar way, the following equations can be obtained, according to Fig. 6 (a) and (b) and the volt-second balance principle on inductors L_1 and L_2:

$$\begin{cases} d_{\text{Buck}} \cdot (U_{\text{C4}} - U_{\text{C2}} - U_{\text{low}}) + (1-d_{\text{Buck}}) \cdot (-U_{\text{low}}) = 0 \\ d_{\text{Buck}} \cdot (U_{\text{C4}} - U_{\text{C1}}) + (1-d_{\text{Buck}}) \cdot (-(U_{\text{C5}} + U_{\text{C1}}) + U_{\text{C3}}) = 0 \end{cases} \tag{6}$$

$$\begin{cases} U_{\text{C4}} + U_{\text{C5}} = U_{\text{high}} \\ U_{\text{C2}} + U_{\text{C5}} = U_{\text{C3}} \\ U_{\text{C3}} = U_{\text{C4}} \\ U_{\text{C1}} = U_{\text{C5}} \end{cases} \tag{7}$$

where d_{Buck} is the duty cycle of Q_2, Q_3 and Q_5 of the proposed converter in the step-down mode.

Therefore, by simplifying (6) and (7), the voltage stresses across C_1-C_5 in the step-down mode can be obtained as:

$$\begin{cases} U_{\text{C1\_Buck}} = U_{\text{C5\_Buck}} = \dfrac{U_{\text{low}}}{d_{\text{Buck}}} = \dfrac{U_{\text{high}}}{3-d_{\text{Buck}}} \\ U_{\text{C2\_Buck}} = \dfrac{(1-d_{\text{Buck}})U_{\text{low}}}{d_{\text{Buck}}} = \dfrac{(1-d_{\text{Buck}})U_{\text{high}}}{3-d_{\text{Buck}}} \\ U_{\text{C3\_Buck}} = U_{\text{C4\_Buck}} = \dfrac{(2-d_{\text{Buck}})U_{\text{low}}}{d_{\text{Buck}}} = \dfrac{(2-d_{\text{Buck}})U_{\text{high}}}{3-d_{\text{Buck}}} \end{cases} \tag{8}$$

and the voltage stresses across Q_1-Q_5 in the step-down mode can also be expressed as:

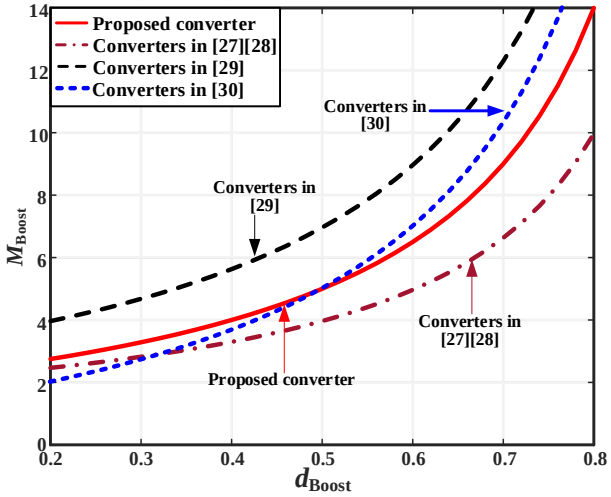
$$\begin{aligned} U_{Q_1\text{\_Buck}} &= U_{Q_2\text{\_Buck}} = U_{Q_3\text{\_Buck}} = U_{Q_4\text{\_Buck}} \\ &= U_{Q_5\text{\_Buck}} = \frac{U_{\text{high}}}{3-d_{\text{Buck}}} = \frac{U_{\text{high}}+U_{\text{low}}}{3} \end{aligned} \tag{9}$$

Substituting (8) into (7), the voltage gain G_{Buck} (in CCM) of the proposed converter in the step-down mode can be expresses as:

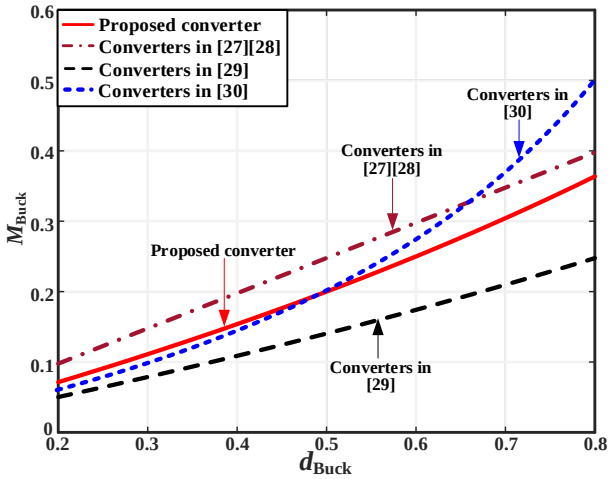
$$G_{\text{Buck}} = \frac{d_{\text{Buck}}}{3-d_{\text{Buck}}} \tag{10}$$

D. Comparisons with Other Converters

Comparisons between the proposed converter and other counterpart converters in CCM, regarding to the voltage gain, the rated output power, the maximum voltage and current stresses across the power switches, the measured maximum efficiencies and the component count, are given in TABLE II. The other four converters mainly include: the bidirectional dc-dc converter in [27], the multiphase converter with two stages in parallel and one multiplier stage in [28], the switched-capacitor-based active network dc-dc converter (SC-ANC) in [29] and the high voltage gain dc-dc converter in [30]. The voltage gain against the duty cycle curves of these five converters in two operating modes are plotted in Fig. 7. According to TABLE II and Fig. 7, the proposed converter has the following advantages:



(a) Step-up mode.



(b) Step-down mode.

Fig. 7 Comparisons of voltage gain against duty cycle.

1) The voltage gain of the proposed converter is higher than those in [27] and [28], but lower than those in [29] and [30], and the proposed converter also has lower voltage stresses compared to those in [27]-[30].

2) In order to improve the voltage gain range, the additional current path through the power switch Q_1 exists, which makes

the maximum current stress across Q_1 little bit higher than others.

3) The proposed converter has a smaller power switch count compared to that in [28], but one larger than those in [27] and [30], and the proposed one also has a slightly higher LC components count compared to those in [27]-[30].

4) The measured maximum efficiencies of the proposed converter are higher than those of the converters in [27] and [28] and close to those of the converter in [30], but lower than those of the converter in [29].

Therefore, the proposed converter gives a good balance among the voltage gain, the components counts and the voltage and current stresses, which gives a viable solution to the application of the hybrid energy sources EVs focused in the paper.

TABLE II
COMPARISONS BETWEEN THE PROPOSED CONVERTER AND OTHER CONVERTERS

Topologies		Proposed converter	Converter in [27]	Converter in [28]	Converter in [29]	Converter in [30]
Voltage gain	Step-up	$(2+d_{Boost})/(1-d_{Boost})$	$2/(1-d_{Boost})$	$2/(1-d_{Boost})$	$(3+d_{Boost})/(1-d_{Boost})$	$(1+3d_{Boost})/(1-d_{Boost})$
	Step-down	$d_{Buck}/(3-d_{Buck})$	$d_{Buck}/2$	$d_{Buck}/2$	$d_{Buck}/(4-d_{Buck})$	$d_{Buck}/(4-3d_{Buck})$
Rated output power		400W	500W	400W	200W	200W
Max voltage stress across power switches		$(U_{high}+U_{low})/3$	U_{high}	U_{high}	$(U_{high}+U_{low})/2$	$(U_{high}+3U_{low})/2$
Max current stress across power switches		$(1+2d_{Boost})I_{high}/(d_{Boost}(1-d_{Boost}))$	$I_{high}/(1-d_{Boost})$	$2I_{high}/(1-d_{Boost})$	$(3-d_{Boost})I_{high}/(1-d_{Boost})$	$2I_{high}/(1-d_{Boost})$
		$(3-2d_{Buck})I_{low}/((3-d_{Buck})(1-d_{Buck}))$	$I_{low}/2$	I_{low}	$(2+d_{Buck})I_{low}/(4-d_{Buck})$	$2I_{low}/(4-3d_{Buck})$
Measured maximum efficiencies		η_{Boost}=94.09%	η_{Boost}=93.86%	η_{Boost}=92.6%	η_{Boost}=97.3%	η_{Boost}=94.27%
		η_{Buck}=94.41%	η_{Buck}=93.40%	/	/	/
Count of power switch		5	4	6	5	4
Count of capacitor		6	3	4	4	4
Count of inductor		2	2	2	2	3

III. PARAMETER DESIGN OF THE PROPOSED CONVERTER

According to the analysis in Section II, the main parameters of the proposed converter are designed and analyzed in this section.

A. Parameter Design of Power Switches

The parameter design of power switches mainly depends on the voltage and current stresses, and the voltage drops of the power switches are ignored.

1. Voltage Stresses across the Power Switches

The voltage stresses across Q_1-Q_5 in the step-up and step-down modes have been given in (4) and (9), they are all one-third of the sum of U_{high} and U_{low}, which are much lower than those of the conventional converters.

2. Current Stresses across the Power Switches

According to Fig. 4 and Fig. 6, and the Kirchhoff's current law (KCL), the current stresses across Q_1-Q_5 in the step-up and the step-down modes can be obtained as follows:

$$\begin{cases} I_{Q_1\_Boost} = \dfrac{1+2d_{Boost}}{d_{Boost}(1-d_{Boost})} I_{high} \\ I_{Q_2\_Boost} = I_{Q_3\_Boost} = I_{Q_5\_Boost} = \dfrac{1}{1-d_{Boost}} I_{high} \\ I_{Q_4\_Boost} = \dfrac{1}{d_{Boost}} I_{high} \end{cases} \tag{11}$$

$$\begin{cases} I_{Q_1\_Buck} = \dfrac{3-2d_{Buck}}{(3-d_{Buck})(1-d_{Buck})} I_{low} \\ I_{Q_2\_Buck} = I_{Q_3\_Buck} = I_{Q_5\_Buck} = \dfrac{1}{3-d_{Buck}} I_{low} \\ I_{Q_4\_Buck} = \dfrac{d_{Buck}}{(3-d_{Buck})(1-d_{Buck})} I_{low} \end{cases} \tag{12}$$

where d_{Boost}=1-d_{Buck}. Therefore, the current stress across Q_1 is higher than those of Q_2-Q_5 both in the step-up and step-down modes.

As to selecting the power switches (MOSFETs) for converters, it is always limited by the voltage stresses across the power switches, while the current stresses across the power switches are easy to meet. As Q_1-Q_5 have the same voltage stresses, the identical type of power switches can be selected.

B. Parameter Design of Inductors

The parameter design of the inductors mainly depends on the rated voltage and current, the duty cycle d_{Boost} or d_{Buck}, the permitted fluctuation range x_L% and the switching frequency f_s of the proposed converter. According to Fig. 4 and Fig. 6 and the ampere-second balance principle on C_1-C_5, the rated currents of L_1 and L_2 in the step-up and step-down modes can be obtained as follows:

$$\begin{cases} I_{L1} = \dfrac{2+d_{Boost}}{1-d_{Boost}} I_{high} \\ I_{L2} = I_{high} \end{cases} \tag{13}$$

$$\begin{cases} I_{L1} = I_{low} \\ I_{L2} = \dfrac{d_{Buck}}{3-d_{Buck}} I_{low} \end{cases} \tag{14}$$

Therefore, the minimum values of inductors L_1 and L_2 in the step-up and step-down modes are expressed as follows:

$$\begin{cases} L_1 \geq \dfrac{U_{low} \times (1-d_{Boost}) \times d_{Boost}}{(2+d_{Boost}) \times f_s \times I_{high} \times x_{L1}\%} \\ L_2 \geq \dfrac{U_{low} \times d_{Boost}}{f_s \times I_{high} \times x_{L2}\%} \end{cases} \tag{15}$$

$$\begin{cases} L_1 \geq \dfrac{U_{high} \times (1-d_{Buck}) \times d_{Buck}}{(3-d_{Buck}) \times f_s \times I_{low} \times x_{L1}\%} \\ L_2 \geq \dfrac{U_{high} \times (1-d_{Buck})}{f_s \times I_{low} \times x_{L2}\%} \end{cases} \tag{16}$$

C. Parameter Design of Capacitors

The parameter design of the capacitors mainly depends on the root mean square (RMS) capacitor currents, the rated voltage and current, the duty cycle d_{Boost} or d_{Buck}, the permitted fluctuation range x_C% and the switching frequency f_s of the proposed converter. According to Fig. 4 and Fig. 6, and the Kirchhoff's current law (KCL), the RMS currents of capacitors C_1-C_5 in the step-up and the step-down modes can be obtained as follows:

$$\begin{cases} I_{C1\_RMS} = \sqrt{\dfrac{d_{Boost}}{1-d_{Boost}}} I_{high} \\ I_{C2\_RMS} = (1+d_{Boost}) \sqrt{\dfrac{1}{d_{Boost}(1-d_{Boost})}} I_{high} \\ I_{C3\_RMS} = \sqrt{\dfrac{1}{d_{Boost}(1-d_{Boost})}} I_{high} \\ I_{C4\_RMS} = \sqrt{\dfrac{d_{Boost}}{1-d_{Boost}}} I_{high} \\ I_{C5\_RMS} = \sqrt{\dfrac{1-d_{Boost}}{d_{Boost}}} I_{high} \end{cases} \quad (17)$$

$$\begin{cases} I_{C1\_RMS} = \dfrac{1}{3-d_{Buck}} \sqrt{d_{Buck}(1-d_{Buck})} I_{low} \\ I_{C2\_RMS} = \dfrac{2-d_{Buck}}{3-d_{Buck}} \sqrt{\dfrac{d_{Buck}}{(1-d_{Buck})}} I_{low} \\ I_{C3\_RMS} = \dfrac{1}{3-d_{Buck}} \sqrt{\dfrac{d_{Buck}}{(1-d_{Buck})}} I_{low} \\ I_{C4\_RMS} = \dfrac{1}{3-d_{Buck}} \sqrt{d_{Buck}(1-d_{Buck})} I_{low} \\ I_{C5\_RMS} = \dfrac{d_{Buck}}{3-d_{Buck}} \sqrt{\dfrac{d_{Buck}}{(1-d_{Buck})}} I_{low} \end{cases} \quad (18)$$

where I_{Ck_RMS} (k=1, 2…5) are the RMS currents of capacitors C_1-C_5. According to (17), (18) and the rated experimental parameters, the RMS capacitor currents are all smaller than the current of the low voltage side, so the maximum power level of the proposed converter will not be limited by them.

Meanwhile, the rated voltages of the capacitors can be obtained from (3) and (8). Hence, the minimum values of capacitors C_1-C_5 in the step-up and step-down modes can be derived as follows:

$$\begin{cases} C_1 \ge \dfrac{(1-d_{Boost}) \times I_{C1off}}{U_{C1} \times x_{C1}\% \times f_s} = \dfrac{d_{Boost} \times (1-d_{Boost}) \times I_{high}}{U_{low} \times x_{C1}\% \times f_s} \\ C_2 \ge \dfrac{(1-d_{Boost}) \times I_{C2off}}{U_{C2} \times x_{C2}\% \times f_s} = \dfrac{(1+d_{Boost}) \times (1-d_{Boost}) \times I_{high}}{d_{Boost} \times U_{low} \times x_{C2}\% \times f_s} \\ C_3 \ge \dfrac{(1-d_{Boost}) \times I_{C3off}}{U_{C3} \times x_{C3}\% \times f_s} = \dfrac{(1-d_{Boost}) \times I_{high}}{(1+d_{Boost}) \times U_{low} \times x_{C3}\% \times f_s} \\ C_4 \ge \dfrac{(1-d_{Boost}) \times I_{C4off}}{U_{C4} \times x_{C4}\% \times f_s} = \dfrac{d_{Boost} \times (1-d_{Boost}) \times I_{high}}{(1+d_{Boost}) \times U_{low} \times x_{C4}\% \times f_s} \\ C_5 \ge \dfrac{(1-d_{Boost}) \times I_{C5off}}{U_{C5} \times x_{C5}\% \times f_s} = \dfrac{(1-d_{Boost})^2 \times I_{high}}{U_{low} \times x_{C5}\% \times f_s} \end{cases} \quad (19)$$

$$\begin{cases} C_1 \ge \dfrac{d_{Buck} \times I_{C1on}}{U_{C1} \times x_{C1}\% \times f_s} = \dfrac{d_{Buck} \times (1-d_{Buck}) \times I_{low}}{U_{high} \times x_{C1}\% \times f_s} \\ C_2 \ge \dfrac{d_{Buck} \times I_{C2on}}{U_{C2} \times x_{C2}\% \times f_s} = \dfrac{(2-d_{Buck}) \times d_{Buck} \times I_{low}}{(1-d_{Buck}) \times U_{high} \times x_{C2}\% \times f_s} \\ C_3 \ge \dfrac{d_{Buck} \times I_{C3on}}{U_{C3} \times x_{C3}\% \times f_s} = \dfrac{d_{Buck} \times I_{low}}{(2-d_{Buck}) \times U_{high} \times x_{C3}\% \times f_s} \\ C_4 \ge \dfrac{d_{Buck} \times I_{C4on}}{U_{C4} \times x_{C4}\% \times f_s} = \dfrac{d_{Buck} \times I_{low}}{2 \times (2-d_{Buck}) \times U_{high} \times x_{C4}\% \times f_s} \\ C_5 \ge \dfrac{d_{Buck} \times I_{C5on}}{U_{C5} \times x_{C5}\% \times f_s} = \dfrac{d_{Buck} \times I_{low}}{2 \times U_{high} \times x_{C5}\% \times f_s} \end{cases} \quad (20)$$

D. Dynamic Modelling Analysis and Voltage Control Scheme

It is assumed that the inductor currents $i_{L1}(t)$ and $i_{L2}(t)$, the capacitor voltages $u_{C1}(t)$-$u_{C5}(t)$ are the state variables, and the power switches, the inductors and the capacitors are all in the ideal condition. The capacitor currents $i_{C1}(t)$-$i_{C5}(t)$ are mutually coupled, and there are two invalid state variables. By considering the equivalent series resistances (e.g. R_{C1}=0.01Ω for C_1 and R_{C3}=0.01Ω for C_3), the coupling between the capacitors C_1-C_5 can be removed to avoid the invalid state variables. When the ripples of the inductor current and the capacitor voltage are neglected, the small signal AC equation of the proposed converter in the step-up mode can be derived as (21) with the state space averaging method, shown at the top of the next page.

According to (21) and the experimental parameters in TABLE III, the control-to-output transfer function of the proposed converter in the step-up mode can be achieved from the time domain to the complex frequency domain as (22), shown at the top of the next page.

Similarly, the control-to-output transfer function of the proposed converter in the step-down mode can also be achieved from the time domain to the complex frequency domain with the state space averaging method as (23), shown at the top of the next page.

In order to make the proposed converter achieve the better output voltage performance, an output voltage loop is adopted, and the voltage control scheme can be shown in Fig. 8, where $G_{uod}(s)$ is the transfer function of the proposed converter, $G_m(s)$ is the transfer function of the pulse-width modulator, $H(s)$ is the feedback transfer function, and $G_c(s)$ is the voltage controller (i.e. a PI (Proportional-Integral) controller) transfer function, as shown in (24). In the closed-loop system of the proposed converter, the transfer functions $G_m(s)$=1, $H(s)$=1 are unitized. Therefore, the voltage controller can be designed for the proposed converter to achieve better performance.

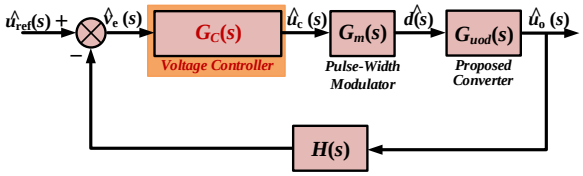


Fig. 8 Voltage control scheme of the proposed converter.

$$\begin{bmatrix} \frac{\mathrm{d}\hat{i}_{L1}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}\hat{i}_{L2}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}\hat{u}_{C1}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}\hat{u}_{C2}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}\hat{u}_{C3}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}\hat{u}_{C4}(t)}{\mathrm{d}t} \\ \frac{\mathrm{d}\hat{u}_{C5}(t)}{\mathrm{d}t} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{1-D}{L_1} & 0 & -\frac{1-D}{L_1} & 0 \\ 0 & -\frac{DR_{C1}}{L_2} & \frac{D}{L_2} & -\frac{1}{L_2} & 0 & 0 & 0 \\ 0 & -\frac{D}{C_1} & -\frac{1-D}{C_1R_{C1}} & -\frac{1-D}{C_1R_{C1}} & 0 & \frac{1-D}{C_1R_{C1}} & 0 \\ -\frac{1-D}{C_2} & \frac{1}{C_2} & -\frac{1-D}{C_2R_{C1}} & -\frac{1}{C_2}(\frac{D}{R_{C3}}+\frac{1-D}{R_{C1}}) & \frac{D}{C_2R_{C3}} & \frac{1-D}{C_2R_{C1}} & -\frac{D}{C_2R_{C3}} \\ 0 & 0 & 0 & \frac{D}{C_3R_{C3}} & -\frac{1}{C_3R_{C3}} & \frac{1-D}{C_3R_{C3}} & \frac{D}{C_3R_{C3}} \\ \frac{1-D}{C_4} & 0 & \frac{1-D}{C_4R_{C1}} & \frac{1-D}{C_4R_{C1}} & \frac{1-D}{C_4R_{C3}} & -\frac{1}{C_4R}-\frac{1-D}{C_4}(\frac{1}{R_{C1}}+\frac{1}{R_{C3}}) & -\frac{1}{C_4R} \\ 0 & 0 & 0 & -\frac{D}{C_5R_{C3}} & \frac{D}{C_5R_{C3}} & -\frac{1}{C_5R} & -\frac{1}{C_5}(\frac{1}{R}+\frac{D}{R_{C3}}) \end{bmatrix} \begin{bmatrix} \hat{i}_{L1}(t) \\ \hat{i}_{L2}(t) \\ \hat{u}_{C1}(t) \\ \hat{u}_{C2}(t) \\ \hat{u}_{C3}(t) \\ \hat{u}_{C4}(t) \\ \hat{u}_{C5}(t) \end{bmatrix}$$

$$+\begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \hat{u}_{\mathrm{low}}(t) + \begin{bmatrix} 0 & 0 & 0 & -\frac{1}{L_1} & 0 & \frac{1}{L_1} & 0 \\ 0 & -\frac{R_{C1}}{L_2} & \frac{1}{L_2} & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{C_1} & \frac{1}{C_1R_{C1}} & \frac{1}{C_1R_{C1}} & 0 & -\frac{1}{C_1R_{C1}} & 0 \\ \frac{1}{C_2} & 0 & \frac{1}{C_2R_{C1}} & \frac{1}{C_2}(\frac{1}{R_{C1}}-\frac{1}{R_{C3}}) & \frac{1}{C_2R_{C3}} & -\frac{1}{C_2R_{C1}} & -\frac{1}{C_2R_{C3}} \\ 0 & 0 & 0 & \frac{1}{C_3R_{C3}} & 0 & -\frac{1}{C_3R_{C3}} & \frac{1}{C_3R_{C3}} \\ -\frac{1}{C_4} & 0 & -\frac{1}{C_4R_{C1}} & -\frac{1}{C_4R_{C1}} & -\frac{1}{C_4R_{C3}} & \frac{1}{C_4}(\frac{1}{R_{C1}}+\frac{1}{R_{C3}}) & 0 \\ 0 & 0 & 0 & -\frac{1}{C_5R_{C3}} & \frac{1}{C_5R_{C3}} & 0 & -\frac{1}{C_5R_{C3}} \end{bmatrix} \begin{bmatrix} I_{L1} \\ I_{L2} \\ U_{C1} \\ U_{C2} \\ U_{C3} \\ U_{C4} \\ U_{C5} \end{bmatrix} \hat{d}(t) \quad (21)$$

$$\hat{u}_{\mathrm{high}}(t) = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} \hat{i}_{L1}(t) & \hat{i}_{L2}(t) & \hat{u}_{C1}(t) & \hat{u}_{C2}(t) & \hat{u}_{C3}(t) & \hat{u}_{C4}(t) & \hat{u}_{C5}(t) \end{bmatrix}^{\mathrm{T}}$$

$$G_{u_{\mathrm{high}}d_{\mathrm{Boost}}}(s) = \frac{\hat{u}_{\mathrm{high}}(s)}{\hat{d}_{\mathrm{Boost}}(s)} = \frac{-1.9\times10^{4}s^{6} - 1.3\times10^{10}s^{5} - 1.2\times10^{15}s^{4} - 3.4\times10^{19}s^{3} - 2.3\times10^{23}s^{2} - 2.9\times102^{5}s + 7.1\times10^{29}}{s^{7} + 6.8\times10^{5}s^{6} + 1.1\times10^{11}s^{5} + 3.1\times10^{15}s^{4} + 5.0\times10^{17}s^{3} + 1.1\times10^{22}s^{2} + 7.1\times10^{22}s + 4.4\times10^{26}} \quad (22)$$

$$G_{u_{\mathrm{low}}d_{\mathrm{Buck}}}(s) = \frac{\hat{u}_{\mathrm{low}}(s)}{\hat{d}_{\mathrm{Buck}}(s)} = \frac{7.8\times10^{8}s^{6} + 8.3\times10^{14}s^{5} + 2.5\times10^{20}s^{4} + 2.2\times10^{25}s^{3} + 4.6\times10^{29}s^{2} + 9.2\times10^{31}s + 1.5\times10^{36}}{s^{8} + 1.1\times10^{6}s^{7} + 3.3\times10^{11}s^{6} + 2.8\times10^{16}s^{5} + 6.1\times10^{20}s^{4} + 5.8\times10^{23}s^{3} + 5.0\times10^{27}s^{2} + 1.5\times10^{30}s + 9.4\times10^{33}} \quad (23)$$

$$G_{\mathrm{c}}(s) = K_{\mathrm{p}} + K_{\mathrm{i}}\frac{1}{s} \quad (24)$$

where $K_{\mathrm{p\_Boost}}$=0.0001, and $K_{\mathrm{i\_Boost}}$=0.0002 in the step-up mode, and $K_{\mathrm{p\_Buck}}$=0.05, and $K_{\mathrm{i\_Buck}}$=0.001 in the step-down mode, which are used in the experiments.

IV. Experimental Results and Analysis

A 400W scaled-down prototype with U_{high}=400V and U_{low}=40~120V is built to verify the operating principle of the proposed converter, as shown in Fig. 9. The experimental parameters of the experimental prototype are shown in TABLE III. The switching frequency of the proposed converter is selected as 20 kHz after the trade-off between the power density and the efficiency, and a Texas Instruments digital signal processor (DSP) TMS32028335 is employed for the voltage loop controller.

TABLE III
Experimental Parameters of the Converter

Parameter	Values
Filtering capacitor: C_{low}	470μF
Switched capacitors: C_1-C_5	520μF
Inductor 1: L_1	400μH
Inductor 2: L_2	600μH
Switching frequency: f_{s}	20kHz
Voltage loop controller	TMS32028335
Power MOSFETs: Q_1~Q_5	IXTH88N30P

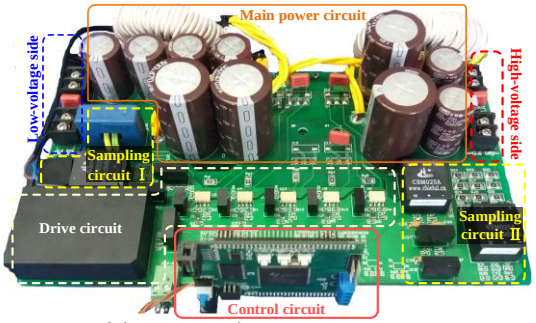
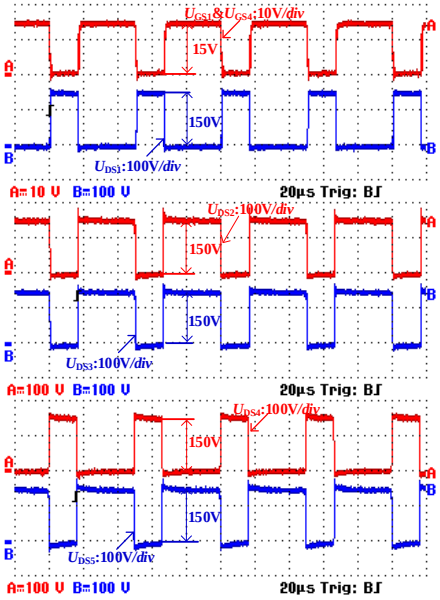


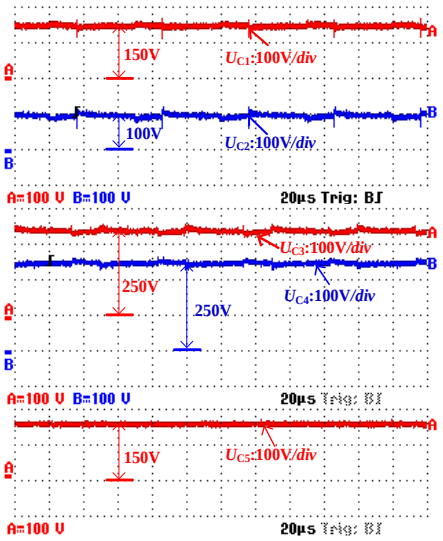
Fig. 9 Prototype of the proposed converter.

A. Experimental Results in Two Operating Modes

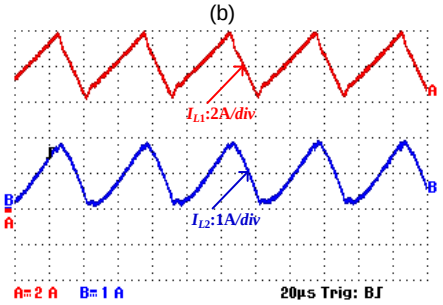
The voltage and current waveforms of the main electrical components of the proposed converter in the step-up and step-down modes are shown in Fig. 10 and Fig. 11 respectively. As shown in Fig. 10 (a) and Fig. 11 (a), the voltage stresses across Q_1-Q_5 are 150V (i.e. one-third of the sum of the high-side and low-side voltages), which are consistent with (4) and (9). Fig. 10 (b) and Fig. 11 (b) show the voltage stresses across C_1-C_5. It can be seen that the voltage stresses across C_1-C_5 are also consistent with (3) and (8). The current waveforms of L_1 and L_2 are shown in Fig. 10 (c) and Fig. 11 (c). It can be seen that the average currents of inductors L_1 and L_2 are about 8A and 1A, and the current ripples of L_1 and L_2 are about 50% and 200% respectively, which satisfy the theoretical calculations and the design requirements. In order to emulate the charging and discharging processes of the low voltage source, Fig. 10 (d) and Fig. 11 (d) illustrate the dynamic responses of the output and the input voltages when U_{low} varies between 40V and 120V continuously, and also validate that the proposed converter can obtain a wide voltage gain range in both step-up and step-down modes. As shown in these figures, the voltage and current waveforms of the electrical components validate the steady-state analysis and parameters design in Section II and Section III.



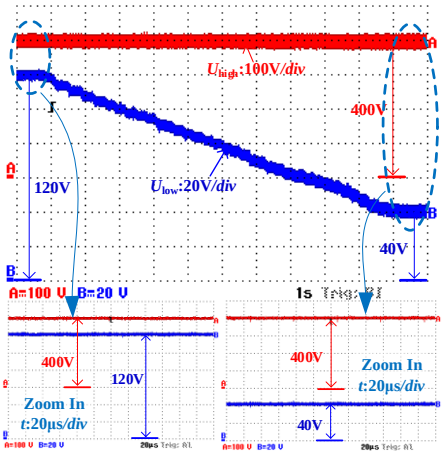
(a)



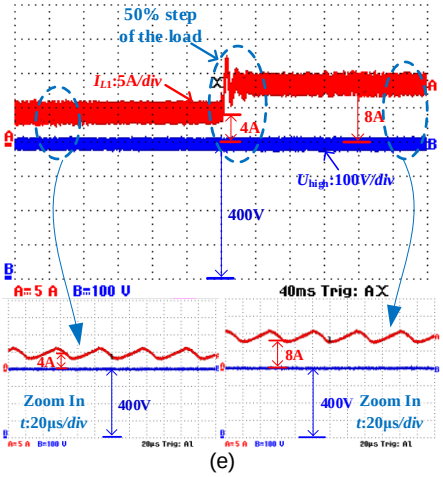
(b)



(c)



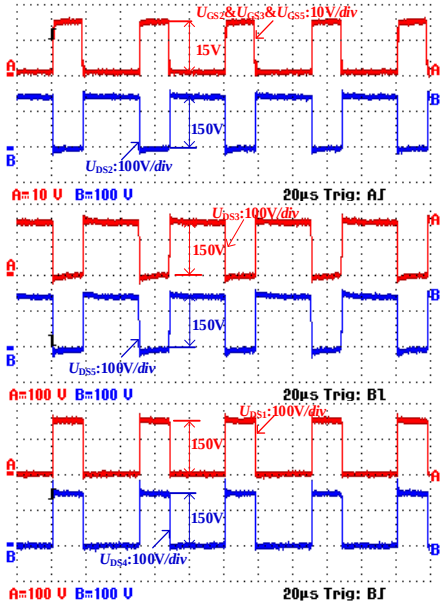
(d)



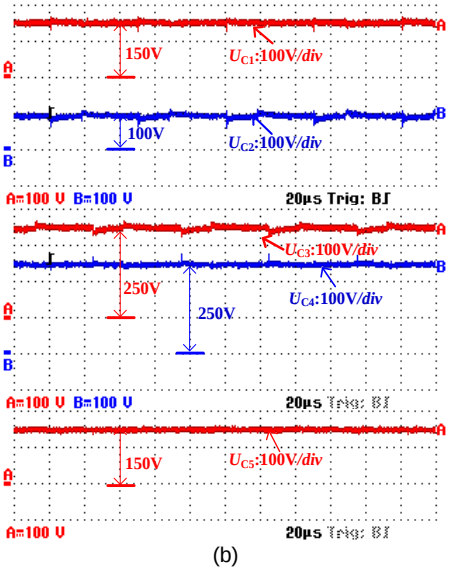
(e)

Fig. 10 Experimental results of the proposed converter in the step-up mode.
(a) Voltage stresses across Q_1-Q_5. (b) Voltage stresses across C_1-C_5.
(c) Inductor currents I_{L1} and I_{L2}. (d) Input voltage U_{low} and output voltage U_{high} when U_{low} varies from 120V to 40V.
(e) Output voltage U_{high} and inductor current i_{L1} when output power P_o is step changed from 200W to 400W.

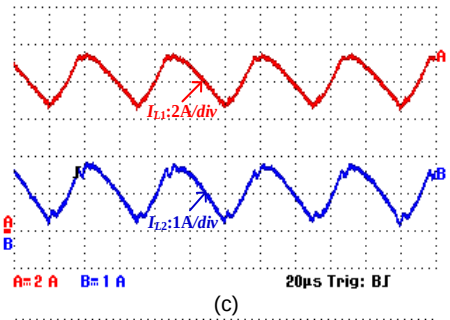
Meanwhile, the output voltage and the inductor current i_{L1} are shown in Fig. 10 (e) and Fig. 11 (e), when the output power P_o is step changed from 200W to 400W in the step-up and step-down modes. It can be seen that when the proposed converter operates under the output voltage closed-loop control, the output voltage can nearly be maintained at the reference voltage and its fluctuation is negligible. The inductor current i_{L1} can also respond quickly according to the sudden change of the load, and the response time of the voltage controller is less than 40ms. Therefore, the proposed converter can achieve a better dynamic and static performance. Moreover, it can be seen from the counterparts which are zoomed in in Fig. 10 (d) (e) and Fig. 11 (d) (e), the fluctuation of the experimental output voltage is less than 2% when the input/output voltages and the load are changing.



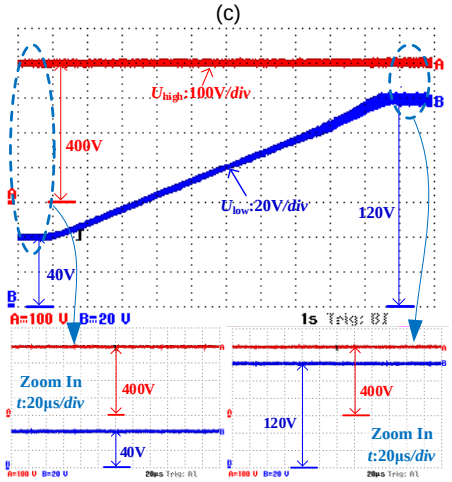
(a)



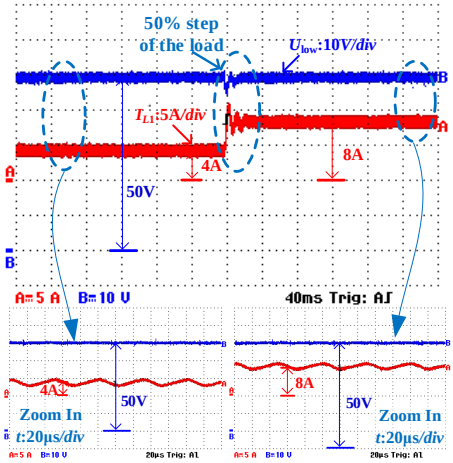
(b)



(c)



(d)



(e)

Fig. 11 Experimental results of the proposed converter in the step-down mode.
(a) Voltage stresses across Q_1-Q_5. (b) Voltage stresses across C_1-C_5.
(c) Inductor currents I_{L1} and I_{L2}. (d) Output voltage U_{low} and input voltage U_{high} when U_{low} varies from 40V to 120V.
(e) Output voltage U_{low} and inductor current i_{L1} when output power P_o is step changed from 200W to 400W.

B. Experimental Result of Bidirectional Power Flow

When the proposed bidirectional dc-dc converter interfaces the high voltage dc bus and the low voltage super-capacitor bank in the hybrid energy sources system, as shown in Fig. 2, the waveforms of i_{Bat} and i_{SC} during the mutation in dc bus load are shown in Fig. 12.

According to Fig. 12, when the dc bus demanded power is stable at 450W or 650W, almost the full power is supplied by the battery pack, and the super-capacitor bank only plays the role of stabilizing the dc bus voltage. However, when the power required by the dc bus p_{Bus} varies between 450W and 650W, the proposed bidirectional dc-dc converter responds quickly and

operates in the step-up or step-down mode, and the instantaneous power of the peak shaving and valley filling is provided or absorbed by the super-capacitor bank through the proposed dc-dc converter, avoiding the step change current from or into the battery pack. The power $|\Delta P|$ of the peak shaving and valley filling is less than the rated power P_N of the proposed converter (e.g., $|\Delta P|$=650W-450W=200W<P_N= 400W). Therefore, the proposed converter is able to operate in both step-up and step-down modes, and the super-capacitor bank and the battery pack of the hybrid energy sources system can be fully used, so as to improve the static and dynamic response of the whole system.

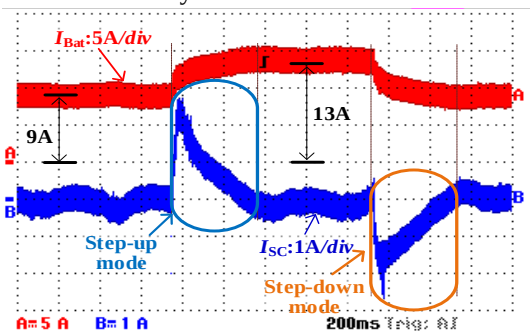


Fig. 12 Experimental result of bidirectional power flow.

C. Efficiency Analysis of the Proposed Converter

The efficiencies of the proposed converter related to the different voltage gains and output powers (e.g., P_o=200W and 400W) are measured by a power analyzer (YOKOGAWA-WT3000) and illustrated in Fig. 13.

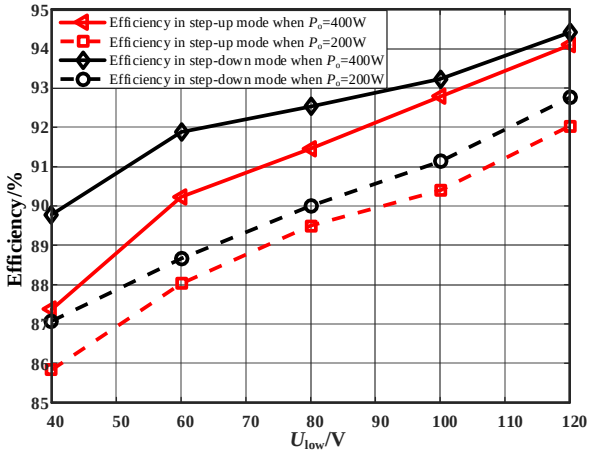


Fig. 13 Efficiency of the proposed converter in step-up and step-down modes when P_o=400W and 200W (U_{high}=400V, U_{low}=40~120V).

As shown in Fig. 13, when the proposed converter operates in the step-up mode, the maximum efficiencies reach 94.09% and 92.03%, and the minimum efficiencies are 87.37% and 85.83%, respectively, when the output power P_o=400W and 200W. Meanwhile, when the proposed converter operates in the step-down mode, the maximum efficiencies reach 94.41% and 92.76%, and the minimum efficiencies are 89.78% and 87.08%, respectively, when the output power P_o=400W and 200W. As shown in Fig. 13, with the increasing of the low-side voltage, the efficiencies of the proposed converter increase gradually, due to the decreasing losses caused by the decreasing input current. Additionally, when the output power P_o of the proposed converter is 400W, the measured efficiencies of the proposed converter in the step-up and step-down modes are higher than those of the proposed converter when P_o is 200W. Meanwhile, the proposed converter can further improve the efficiencies and be well suitable for higher power applications by selecting the power switches (such as SiC MOSFETs) with the better performance. Besides, the improved circuit layout and the better component design can be employed to reduce the circuit parasitic parameters and improve the efficiencies.

V. Conclusion

In this paper, a novel hybrid switched-capacitor/switched -quasi-Z-source bidirectional dc-dc converter with a wide voltage gain range for EVs with the hybrid energy sources has been proposed. The proposed converter has a simple structure and lower voltage stresses across the power switches, which are only one-third of the sum of the high-side and low-side voltages. Its control scheme is also relatively simple and easy to implement. Meanwhile, the operating principle, the voltage and current stresses across the power switches and the comparisons with other converters are analyzed in detail. Besides, the parameter design of the main components, the dynamic modelling analysis and the voltage control scheme are also given. The final experimental results validate the feasibility of the proposed converter. Therefore, for the application of the hybrid energy sources EVs described in the paper, the proposed converter is a viable solution and has a good dynamic and static performance, which provides a good balance among the voltage gain, the components counts and the voltage and current stresses.

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